

1 1. A method for providing a complete end-to-end data
2 path verification in a computer system, the steps comprising:

3 a) providing a data initiator within said computer
4 system;

5 b) providing a data receiver within said computer
6 system and operatively connected to said data
7 initiator over a first data path;

8 c) transmitting a predetermined data test pattern from
9 said data initiator to said data receiver over said
10 first data path;

11 d) receiving said predetermined data test pattern from
12 step (c) at said data receiver;

13 e) transmitting said received data test pattern from
14 step (d) from said data receiver back to said data
15 initiator over a second data path;

16 f) receiving said data test pattern of step (e) at said
17 data initiator; and

18 g) comparing said predetermined data test pattern of
19 step (c) with said data test pattern of step (f).

1 2. The method for providing a complete end-to-end data
2 path verification in a computer system, as recited in claim 1,
3 the steps further comprising:

4 h) indicating an error condition when said
5 predetermined data pattern of step (c) and said data
6 test pattern received from said data receiver if
7 step (f) are different.

1 3. The method for providing a complete end-to-end data
2 path verification in a computer system, as recited in claim 1,
3 the steps further comprising:

4 h) performing a predetermined operation when said
5 predetermined data pattern of step (c) and said data
6 test pattern received from said data receiver if
7 step (f) are different.

1 4. The method for providing a complete end-to-end data
2 path verification in a computer system, as recited in claim 1,
3 wherein said computer system comprises one of the group: a
4 computer and storage router.

1 5. The method for providing a complete end-to-end data
2 path verification in a data system, as recited in claim 4,
3 wherein said computer system comprises a processor and memory
4 operatively connected thereto.

1 6. The method for providing a complete end-to-end data
2 path verification in a computer system, as recited in claim 5,
3 wherein said predetermined data test pattern is stored in said
4 memory.

1 7. The method for providing a complete end-to-end data
2 path verification in a computer system, as recited in claim 6,
3 wherein said computer system further comprises at least one
4 from the group of devices: PCI bus and PCI bridge, SCSI
5 controller, SCSI interface, fibre channel controller, fibre
6 channel interface.

1 8. The method for providing a complete end-to-end data
2 path verification in a computer system, as recited in claim 7,
3 wherein said data path comprises at least one from said group
4 of devices: PCI bus and PCI bridge, SCSI controller, SCSI
5 interface, fibre channel controller, fibre channel interface.

1 9. The method for providing a complete end-to-end data
2 path verification in a computer system, as recited in claim 2,
3 wherein said first data path and said second data path
4 comprise a single data path.

1 10. The method for providing a complete end-to-end data
2 path verification in a computer system, as recited in claim 2,
3 wherein at least one of said transmitting step (c), said
4 receiving step (d), said transmitting step (e) and said
5 receiving step (f) are repeated periodically.

1 11. The method for providing a complete end-to-end data
2 path verification in a computer system, as recited in claim 2,
3 wherein said data initiator comprises a processor within said
4 computer system.

1 12. The method for providing a complete end-to-end data
2 path verification in a computer system, as recited in claim 2,
3 wherein said data receiver comprises at least one of the
4 devices: a SCSI controller, a memory, a fibre channel
5 controller.

2005200438001